MAXIMIZING CAPACITANCE PER UNIT AREA WHILE MINIMIZING SIGNAL TRANSMISSION DELAY IN PCB

BACKGROUND OF THE INVENTION

Field of the Invention

[001] The present invention relates to the field of crosstalk compensation in connectors and, more particularly, to a technique of maximizing capacitance per unit area while minimizing signal transmission delays in crosstalk compensating printed circuit boards (PCBs).

Discussion of the Related Art

[002] Noise or signal interference between conductors in a connector is known as crosstalk. Crosstalk is a common problem in devices using connectors. Particularly, in a system where a modular plug often used with a computer is to mate with a modular jack, the electrical wires (conductors) within the jack and/or plug produce crosstalk.

[003] U.S. Patent No. 5,997,358 issued to Adriaenssens et al. (hereinafter "the '358 patent") describes a multi-stage scheme for compensating crosstalk in connectors. The entire contents of the '358 patent are incorporated by reference. Further, the subject matters of U.S. Patent Nos. 5,915,989; 6,042,427; 6,050,843; and 6,270,381 are also incorporated by reference.

[004] The '358 patent reduces original crosstalk in a modular jack of a connector that receives a plug. The jack includes a PCB with conductors placed on the PCB layers. The original crosstalk between the conductors of the jack is reduced or compensated for by adding a fabricated (compensation) crosstalk at two compensation stages and thereby canceling the crosstalks in the plug-jack combination. The compensation crosstalk is created by placing capacitors on the PCB layers and providing crossed-over conductors at different locations (stages) on the PCB layers.

[005] In such crosstalk compensating systems, it is desirable for the crosstalk compensating PCB to have a high dielectric constant (DK) to minimize the PCB space used to achieve the needed capacitive crosstalk compensation. However, the use of a high DK material for the PCB results in long delays in the signal transmission paths of the conductors between the compensation stages which is detrimental to the high frequency performance of the connector.

[006] Therefore, there exits a need for a technique capable of maximizing an efficient PCB space utilization for the capacitive crosstalk compensation while minimizing signal transmission delays in the PCB.

SUMMARY OF THE INVENTION

[007] The present invention overcomes the problems and limitations of the related art crosstalk compensation devices. Particularly, the present invention provides a crosstalk compensating PCB having some layer(s) made of a high dielectric constant (DK) material and other layers made of a low DK

material. Then the crosstalk compensating capacitors are made to reside at those layers with the high DK material, while other electronic components are made to reside at the layers with the low DK material. This provides the PCB that maximizes the compensating capacitance per unit area while minimizing signal transmission delays.

BRIEF DESCRIPTION OF THE DRAWINGS

[008] The aspects of the invention will be apparent from the following detailed description of the embodiments of the present invention with reference to the accompanying drawings, in which:

[009] Fig. 1 is a cross-sectional view of a crosstalk compensating PCB according to a first embodiment of the present invention;

[010] Fig. 2 is a cross-sectional view of a crosstalk compensating PCB according to a second embodiment of the present invention; and

[011] Fig. 3 is a cross-sectional view of a crosstalk compensating PCB according to a third embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[012] Reference will now be made in detail to the preferred embodiments of the present invention, examples of which are illustrated in the accompanying drawings. In the drawings, same reference numerals are used to indicate same elements.

[013] The present invention provides a multilayer board such as a PCB having different layers with different dielectric constants. Such a board

is used to provide crosstalk compensation. A dielectric constant is a well-known term used to describe the ability of a material to store electrostatic energy. The board includes layer(s) made of a high dielectric constant (DK) material and layers made of a low DK material. Then the crosstalk compensating capacitors are made to reside at those layers with the high DK material, while the other components such as conductors for transmitting signals are made to reside at the layers with the low DK material. This provides the board that maximizes the compensating capacitance per unit area while minimizing signal transmission delays.

[014] Fig. 1 is a cross-sectional view of a crosstalk compensating PCB 10 according to a first embodiment of the present invention.

[015] Referring to Fig. 1, the PCB 10 includes a laminate or core 12, first through fourth prepregs 14, 15, 16 and 17, and a plurality of metalized layers 18 and 19. Prepregs are dielectric material sheets known in the art. A laminate/core is also known, and can be made of a copper clad dielectric material substrate 12a with copper sheets (metalized layers) 12b and 12c formed respectively on top and bottom of the dielectric material substrate 12a. The metalized layers 18 and 19 can be a copper foil or other suitable conductive layer.

[016] The top metalized layer 18, the first prepreg 14 and the second prepreg 15 are stacked up in that order on the top copper sheet 12b of the laminate/core 12. The third prepreg 16, the fourth prepreg 17, and the bottom metalized layer 19 are provided in that order under the bottom copper sheet 12c of the laminate/core 12.

[017] The laminate/core 12 (i.e., the substrate 12a) is made of a high DK material. The first and fourth prepregs 14 and 17 are made of a low DK material. The second and third prepregs 15 and 16 are made of a high DK material.

[018] Because the laminate/core 12 and the second and third prepregs 15 and 16 are made with the high DK material(s), compensation capacitive elements 22 used to compensate for the crosstalk are placed on or as part of the copper sheet(s) 12b and/or 12c of the laminate/core 12 at different compensation stages of the PCB 10. The capacitive elements 22 can be interdigital capacitors or plates of parallel plate capacitors. An interdigital capacitor is a capacitor having a co-planar arrangement of two inter-meshed metal combs each at a different potential, and is known. A parallel plate capacitor is a capacitor composed of two parallel metal plates each at a different potential, and is also known. Moreover the capacitive elements 22 can be buried vias formed as part of the copper sheets 12b and 12c and dielectric material substrate 12a of the laminate/core 12. It is known that a capacitor can be made with two vias each at a different potential. According to this configuration, the needed crosstalk compensation is provided in the PCB 10 by the presence of the compensation capacitive elements 22 and, at the same time, the compensation capacitance per unit area on the PCB 10 is maximized because the high DK PCB layers provide a high capacitance per unit area on the PCB. Furthermore, this configuration provides a compact design for the PCB 10.

[019] Moreover, because the top and bottom metalized layers 18 and 19 are adjacent to the first and fourth prepregs 14 and 17 made with the low DK material(s), circuit elements 20 are placed on or as part of the top and/or bottom metalized layers 18 and 19. The circuit elements 20 are electronic elements primarily used to provide the transmission paths for the signals through the PCB 10. The circuit elements 20 can be conductive traces, resistive elements, inductive elements, etc. The low DK materials surrounding the circuit elements 20 prevent long signal transmission delays as the signals travel along the circuit elements 20, such that they can be transmitted significantly more quickly throughout the PCB 10. As a result, the PCB 10 maximizes the compensation capacitance per unit area while minimizing signal transmission delays in the PCB 10.

[020] Fig. 2 is a cross-sectional view of a crosstalk compensating PCB 30 according to a second embodiment of the present invention. The PCB 30 is identical to the PCB 10 of the first embodiment, except that in the second embodiment, each of the low DK layers as well as the abutting metalized layer is replaced by a laminate/core made of a low DK material, with one of its copper sheets etched out.

[021] Particularly, referring to Fig. 2, the PCB 30 includes the high DK laminate/core 12, the high DK prepreg 15 formed on the laminate/core 12, the high DK prepreg 16 formed under the laminate/core 12, a top laminate/core 32, and a bottom laminate/core 34, all stacked up. in the order as shown in Fig. 2.

[022] The top laminate/core 32 includes a low DK substrate 32a (e.g., a copper clad substrate with a low DK) and only one copper sheet (metalized layer) 32b formed on one side of the low DK substrate 32a. Similarly, the bottom laminate/core 34 includes a low DK substrate 34a (e.g., a copper clad substrate with a low DK) and only one copper sheet (metalized layer) 34b formed on one side of the low DK substrate 34a.

[023] Generally, a laminate/core includes a dielectric material substrate and two copper sheets formed on top and bottom of the substrate. In one implementation, as the top and bottom laminates/cores 32 and 34, a low DK laminate/core that is commercially available can be used by etching out or removing one of the copper sheets from the low DK laminate/core. This reduces the cost of the PCB and simplifies the PCB fabrication process.

[024] Because the laminate/core 12 and the second and third prepregs 15 and 16 are made with the high DK material(s), the compensation capacitive elements 22 are placed on or as part of the copper sheet(s) 12b and/or 12c and/or the dielectric material substrate 12a of the laminate/core 12 at different compensation stages of the PCB 30. According to this configuration, the needed crosstalk compensation is provided in the PCB 30 and, at the same time, the compensation capacitance per unit area on the PCB 30 is maximized because of the presence of the high DK PCB layers surrounding the compensation capacitive elements 22.

[025] Moreover, because the copper sheets 32b and 34b are adjacent to the substrates 32a and 34a made with the low DK material(s), the circuit elements 20 are placed on or as part of the copper sheet(s) 32b and/or 34b.

The low DK materials surrounding the circuit elements 20 prevent long signal transmission delays between the circuit elements 20. As a result, the PCB 30 maximizes the compensation capacitance per unit area while minimizing signal transmission delays in the PCB 30.

[026] Fig. 3 is a cross-sectional view of a crosstalk compensating PCB 50 according to a third embodiment of the present invention. This embodiment is used when it is desired to have the compensation elements reside on the top and/or bottom metalized layers and the signal transmission paths reside on the inner metalized layers of the PCB 50. In this embodiment, instead of having low DK materials at the outer layers of the PCB and having high DK materials at the inner layers of the PCB as in Fig. 1, low DK materials are present at the inner layers of the PCB and high DK materials are present at the outer layers of the PCB.

[027] Particularly, referring to Fig. 3, the PCB 50 includes a laminate/core 50, first through fourth prepregs 54, 55, 56 and 57, and the top and bottom metalized layers 18 and 19, all stacked up as shown in Fig. 3. The laminate/core 50 is composed of a low DK substrate 50a (e.g., a low DK copper clad material substrate) and copper sheets 50b and 50c (metalized layers) formed respectively on top and bottom of the low DK substrate 50a.

[028] The first and fourth prepregs 54 and 57 are made of a high DK material. The second and third prepregs 55 and 56 are made of a low DK material.

[029] Because the prepregs 54 and 57 are made with the high DK material(s), the compensation capacitive elements 22 are placed on or as part of the top and/or bottom metalized layer 18 and/or 19 at different compensation stages of the PCB 50. According to this configuration, the needed crosstalk compensation is provided in the PCB 50 and, at the same time, the compensation capacitance per unit area on the PCB 50 is maximized because of the presence of the high DK PCB layers surrounding the compensation elements 22.

[030] Moreover, because the laminate/core 50 and the prepregs 55 and 56 are made with the low DK material(s), the circuit elements 20 are placed on or as part of the copper sheet(s) 50b and/or 50c. The low DK materials surrounding the circuit elements 20 prevent long signal transmission delays between the circuit elements 20. As a result, the PCB 50 maximizes the compensation capacitance per unit area while minimizing signal transmission delays, when it is desired to have the compensation capacitors/elements reside on the top and/or bottom metalized layers and the signal transmission paths reside on the inner metalized layers in the PCB 50.

[031] In the embodiments of the present invention, a high DK can be in the range of 4.0 to 5.0, and a low DK can be in the range of 2.5 to 3.5. Preferably, a high DK can be at or about 4.5 and a low DK can be at or about 3.0. For instance, in Fig. 1, the laminate/core 12 would have a DK of 4.5, the first and fourth prepregs 14 and 17 would have a DK of 3.0, and the second and third prepregs 15 and 16 would have a DK of 4.5.

[032] Also, in the embodiments of the present invention, as the compensation capacitors 22, various types of capacitors can be used. For instance, interdigital capacitors, parallel plate capacitors, or capacitors formed by buried vias can be used. These elements are known in the art.

[033] Although five PCB substrates (excluding the metalized layers) are illustrated in the drawings, it should be readily apparent that any other number of PCB substrates and/or metalized layers may be used for the PCB. An important aspect is that where the compensation elements 22 are to be placed, a high DK material surrounds them, and where the electronic elements 20 are to be placed, a low DK material surrounds them.

[034] Although the present invention has been explained by the embodiments shown in the drawings described above, it should be understood to the ordinary skilled person in the art that the invention is not limited to the embodiments, but rather that various changes or modifications thereof are possible without departing from the spirit of the invention.